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Improved transconductance multipath recycling folded cascode amplifier

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Abstract
In this paper, an enhanced multipath recycling folded cascode (EMRFC) operational transconductance amplifier (OTA) is presented. In the proposed amplifier a high current node is created in the recycling structure by shorting the two drains of the current mirrors and a positive feedback at the output load are employed with multipath current recycling technique. With these modifications, the proposed amplifier achieves a high DC gain and unity gain bandwidth. The proposed EMRFC amplifier with conventional FC, RFC, and IRFC amplifiers are designed and implemented using UMC 180 nm CMOS technology for a total bias current of 300 μA. The EMRFC amplifier exhibits a DC gain enhancement of about 40 dB as well as a 90 MHz increase in UGB compared to the conventional folded cascode configuration. Moreover, the input-referred noise of the proposed OTA is also reduced. The simulations carried out in Cadence Spectre Environment confirm the theoretical results and illustrate that the proposed amplifier has a better figure of merits (FoMs) compared to its counterparts.

1 Introduction

In many high-speed analog applications like switched capacitive filters, converters, sample and hold circuits, the operational transconductance amplifier (OTA) is the major building block. The performance of the high-speed application depends upon the operational characteristics of the OTA. Hence, in recent times many of the researchers have proposed several techniques for designing these OTAs with wide bandwidth, larger gains, and slew rates with low noise. To deal with the consequences of scaling the technology down to the submicron process and to design high-performance OTAs, folded cascode amplifier is commonly used because of its high DC gain and larger swings.The design equations and processes of a fully differential folded cascode OTA for addressing the needs of inexperienced analogue integrated circuit designers are described in Mallya and Nevin (1989) and considered to be the first of their kind. A transconductance, bandwidth, and slew rate enhancement technique based on current splitting and recycling is proposed in Mottaghi-Kashtiban et al. (2006) and termed as a recycling folded cascode amplifier (RFC) (Assaad and Silva-Martinez 2009). Further improvements in transconductance, unity-gain bandwidth of FC OTA is achieved in Yilei et al. (2012) by employing separate AC and DC paths and is named as improved recycling folded cascode amplifier (IRFC) (Li et al. 2010). The concept of positive feedback for the enhancement in DC gain by increasing the output impedance is utilized and discussed in Akbari et al. (2014). A current steering positive feedback is applied to RFC OTA in Kumaravel and Venkataramani (2014) for performance enhancement in terms of DC gain. The double recycling technique is proposed and adopted to RFC OTA in Yan et al. (2012) and the performance improvements are presented. A novel technique is addressed in Venishetty and Sundaram (2019) for enhancing DC gain by increasing output impedance and termed as modified recycling folded cascode amplifier (MRFC). An FC OTA in which all the transistors are operated in the sub-threshold region for achieving performance metrics with reduced power consumption is described in Ragheb and Kim (2017). High recycling

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folded cascode OTA (HRFC) developed by shorting two drains of the current mirror transistors of recycling structure for enhancing DC gain, unity gain bandwidth is discussed (Yosefi 2019) and the enhanced results are presented in Feizbakhsh and Yosefi (2019). A high current recycling structure including separate AC and DC paths with positive feedback is discussed in Venishetty and Sundaram (2020) and presented simulation results illustrates the enhancements in DC gain, slew rate, and UGB. However depending upon the specifications requirement, several architectures are discussed and designed in (Razavi 2002; Allen and Holberg 2011).

This paper presents a novel multipath recycling technique with the high current node in the recycling structure and positive feedback at the output load for achieving enhancements in the output impedance, transconductance, which leads to achieve high DC gain, and unity-gain bandwidth (UGB).

The proposed paper is organized as follows: Sect. 2 discusses the conventional folded cascode (FC), recycling folded cascode (RFC), and improved recycling folded cascode (IRFC) OTA architectures. Section 3 presents the proposed EMRFC amplifier with detailed analysis for transconductance, output impedance, frequency response, slew rate, and noise using necessary design equations. Section 4 illustrates the simulation results and discussions, while conclusions are presented in Sect. 5.

2 Conventional FC, RFC, and IRFC OTA structures

For understanding the advantages of folded cascode topology, FC OTA and its modified versions RFC and IRFC OTAs are presented here from the state of art literature. Figure 1 illustrates the folded cascode (FC) OTA , while RFC and IRFC are shown in Figs. 2 and 3 respectively. The major limitation of conventional folded cascode OTA shown in Fig. 1 is that the tail current sources M3 and M4 exhibits very high current and do not contribute to the overall transconductance of the OTA. To overcome this limitation at the folded node, modifications are proposed to the conventional FC OTA using current splitting and current recycling techniques, and the new architecture is termed as recycling folded cascode (RFC) OTA (Mottaghi-Kashtiban et al. 2006; Assaad and Silva-Martinez 2009). The current splitting principle is applied by splitting two input transistors M1 and M2 of FC OTA into four M1a, M1b, M2a, and M2b transistors which carry equal currents, while current recycling is implemented by converting tail current sources M3 and M4 of FC OTA into pair of current mirrors with a current-carrying ratios $k : 1$ and is illustrated in Fig. 2. These modifications resulted in the enhancements of transconductance by $(k + 1)/2$ times compared to FC and hence DC gain is also increased with enhanced power efficiency. Further, it is observed from the RFC topology, that the current mirrors formed by splitting input transistors for current recycling use the same path for AC and DC currents. The sharing of the same current path by both AC and DC counterparts has limited the further enhancement of transconductance and also made this technique inefficient for other OTA structures. This limitation of the RFC OTA is resolved by providing separate AC and DC paths in the recycling structure and the new OTA is termed as improved recycling folded cascode (IRFC) amplifier (Yilei et al. 2012; Li et al. 2010) and is illustrated in Fig. 3. As shown in Fig. 3, The transistors M3c-M11b and M4c-M12b carries pure DC currents while AC currents flow through M3a-M3b—M11a and M4a-M4b-M12a. From Mottaghi-Kashtiban et al. (2006);

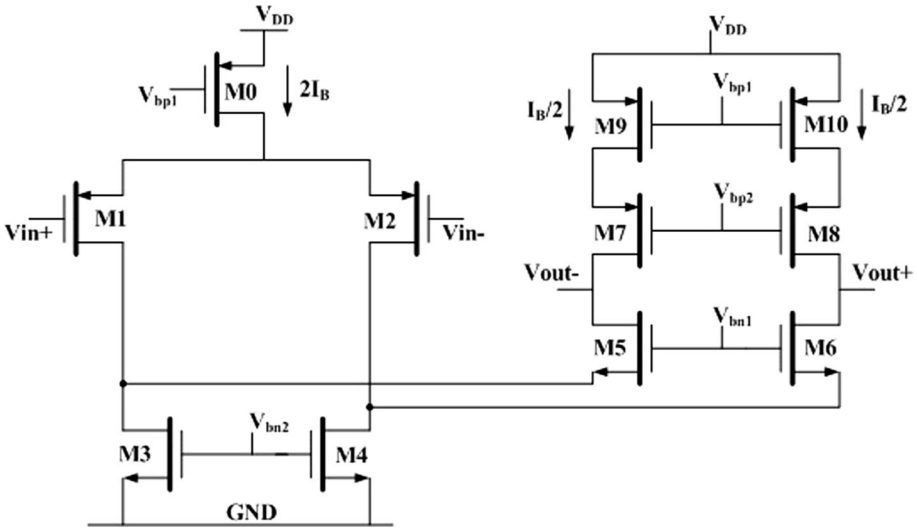

Fig. 1 Fully differential folded cascode amplifier (FC) (Mallya and Nevin 1989)

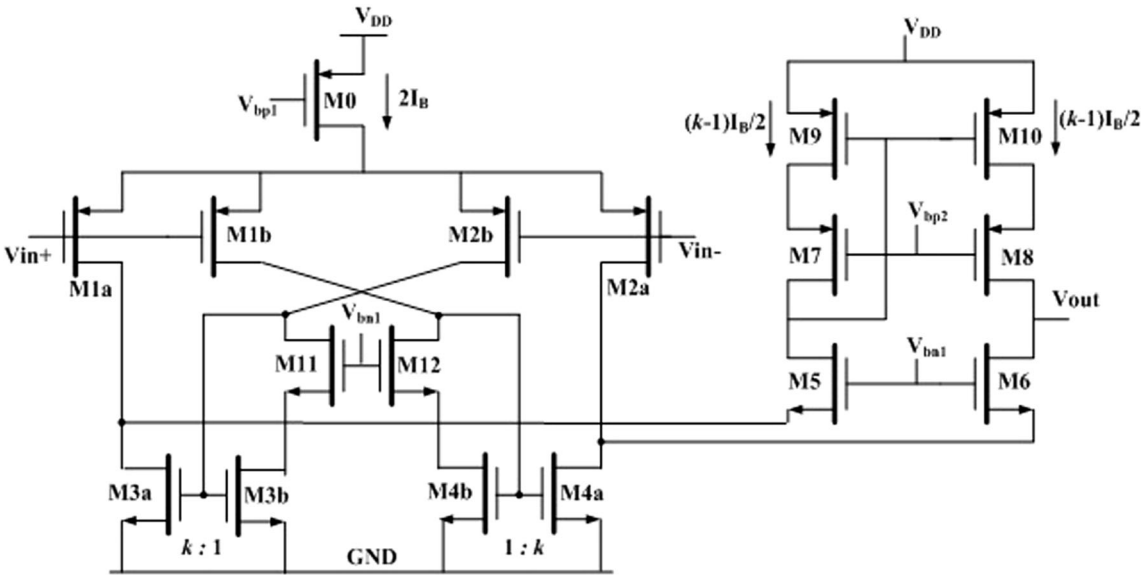

Fig. 2 Recycling folded cascode amplifier (RFC) (Mottaghi-Kashtiban et al. 2006; Assaad and Silva-Martinez 2009)

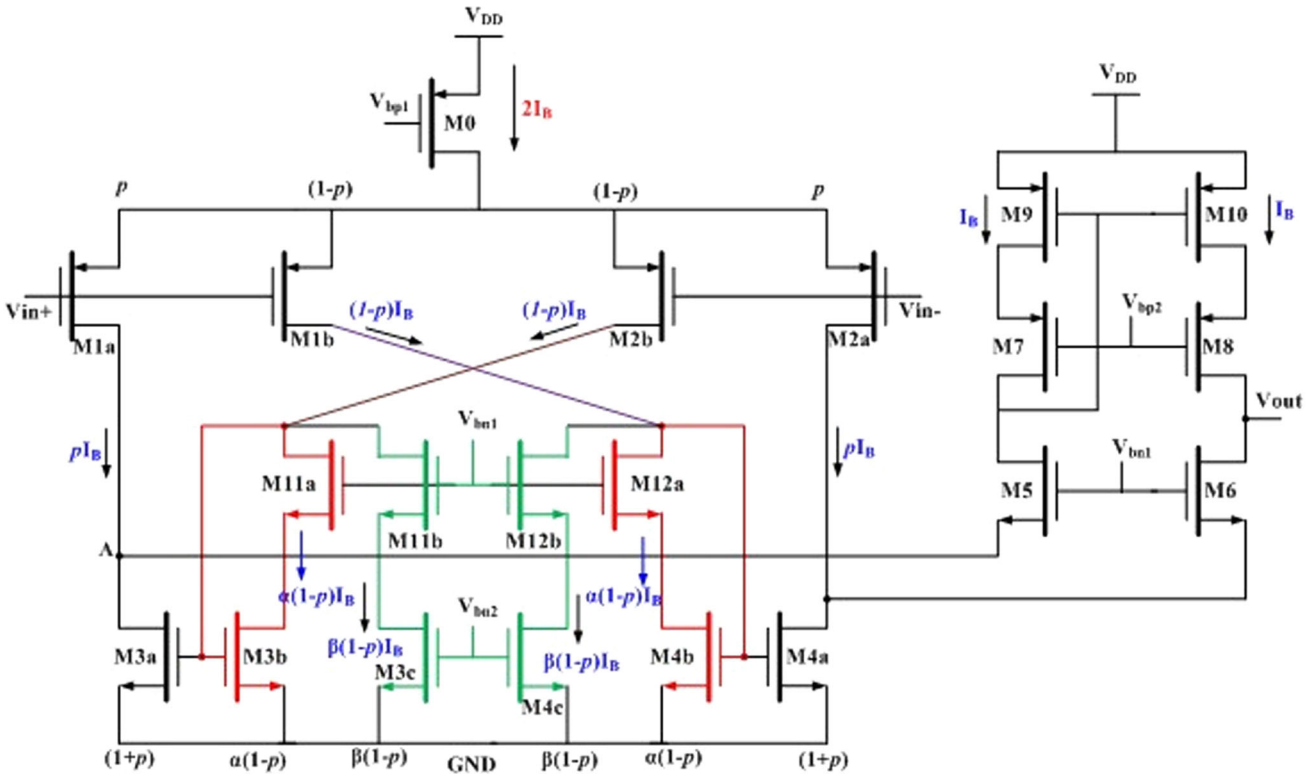

Fig. 3 Improved recycling folded cascode amplifier (IRFC) (Yilei et al. 2012; Li et al. 2010)

Assaad and Silva-Martinez (2009), the effective transconductance (G_m) of FC, RFC, and IRFC OTAs are,

$$G_{m,FC} = g_{m1} \tag{1}$$

$$G_{m,RFC} = (k+1)g_{m1a} \tag{2}$$

$$G_{m,IRFC} = \left(p + \frac{p+1}{\alpha}\right) g_{m1} \tag{3}$$

From Eq. (1), Eq. (2), and Eq. (3),it can be inferred that with proper selection of p and α, IRFC can have improved performance when compared with RFC that achieves 2 times enhancement over FC. Besides its higher

transconductance, IRFC has higher output impedance compared to FC and RFC OTAs, as smaller current flows through M3a and M4a. Hence with improved transconductance and larger output impedance, IRFC exhibits higher DC gain compared to its counterparts FC and RFC.

3 Proposed EMRFC Amplifier

In Yilei et al. (2012) and Li et al. (2010), improved recycling folded cascode amplifier (IRFC) is proposed to enhance the DC gain and unity gain bandwidth of the RFC amplifier by providing separate paths for AC and DC currents. As shown in Fig. 3, the DC path M11b-M3c, M12b-M4c can be utilized further for contributing to overall transconductance by driving the cascode transistors M11b and M12b of DC path from the small-signal inputs and converting the transistors M3c and M4c into a single compound transistor carrying double current compared to IRFC structure. Hence with this modification, the transistors M11b-M12b looks like the input pair of a differential amplifier and the compound transistor acts as a tail current source of the same. To maintain the separate AC and DC path, the transistors M11b and M12b are properly driven with Vin− and Vin+ inputs respectively. Therefore the advantage of achieving enhancement in transconductance by separate AC and DC paths as discussed in IRFC and as well current recycling from the differential pair formed by M11b-M12b can be utilized simultaneously. Hence three small-signal currents flow from folded node to the output, (1) Current flowing to the output from input transistor M1a via M5, (2) Current flowing from another input transistor M2b through the cross over current mirror M3a: M3b through M5 to the output, (3) Recycled current form M12b through current mirror M3a: M3b through M5 to the output. However, it can be observed from the proposed amplifier architecture that the gain of the input differential pair M1b-M2b is remained to be 1, because of diode-connected current mirrors M3b-M11a and M4b-M12a transistors. Also, it can be observed that the transistors M9 and M10 are carrying larger currents but don't contribute to the overall transconductance. Hence the overall transconductance of the amplifier can be further increased by making transistors M3b-M11a, M4b-M12a, and M9-M10 contribute to the gain with the following modifications: 1. Creating a Node 'N' by shorting the drains of the current mirror transistors M3b and M4b. This node is referred to as a High Current Node since it carries twice the current . 2. By incorporating positive feedback at the output by driving the output transistors M9 and M10 with an incremental small signal from the drains of M2b and M1b respectively. Therefore with the principles of multipath current recycling, high current node, and positive feedback, the complete architecture of the proposed amplifier is illustrated in Fig. 4 and is named as Enhanced Multipath Recycling Folded Cascode amplifier (EMRFC). With the proposed architecture, a gain of more than 30 dB is expected compared to FC, RFC, and IRFC amplifiers.

3.1 Performance characteristics of EMRFC

To achieve the maximum advantages of modifications proposed for the enhancements in the performance characteristics, the different current ratios among the transistors in the architecture are maintained properly and the same is illustrated in Fig. 4. The tail current $2I_B$ from M0 is equally distributed among the input transistors M1a-M1b-M2a-M2b, whereas the currents in the current mirror transistors are chosen in the ratios as, M3a: M3b = M4a: M4b = $(1+p):\alpha$. The current flowing from M9 and M10 are $pI_B/2$. The complete analysis of performance characteristics such as transconductance, output impedance, slew rate, and noise with necessary design equations for the proposed amplifier are presented in the following sections.

3.1.1 Small signal transconductance

The effective transconductance ($G_{m,EMRFC}$) of the proposed EMRFC amplifier shown in Fig. 4, can be obtained from the half circuit transistor model depicted in Fig. 5, which includes the effect of high current node N and also multipath recycling principle. Small signal analysis can be performed on the half circuit transistor model. The effective transconductance can be obtained by shorting the output node to ground and finding the expression for the short circuit current (I_{SC}) in terms of input voltage. The node voltage at the gate terminal of the current mirror transistor M3a termed as V_{gs3a}, can be calculated by considering the section of half circuit model shown in Fig. 5 and is illustrated in Fig. 6.

From Fig. 6, the node voltage V_{gs3a} is expressed as,

$$V_{gs3a} = -V_{in}^{-}.(g_{m2b} + g_{m3c})[r_{02b} \parallel r_{03c} \parallel r_{011}] \tag{4}$$

The current flowing through the current mirror transistor M3a (I_{ds3a}) is expressed as,

$$I_{ds3a} = -g_{m3a}.V_{in}^{-}.(g_{m2b} + g_{m3c})[r_{02b} \parallel r_{03c} \parallel r_{011}] \tag{5}$$

Therefore the total short circuit current (I_{SC}) flowing through the output is expressed as,

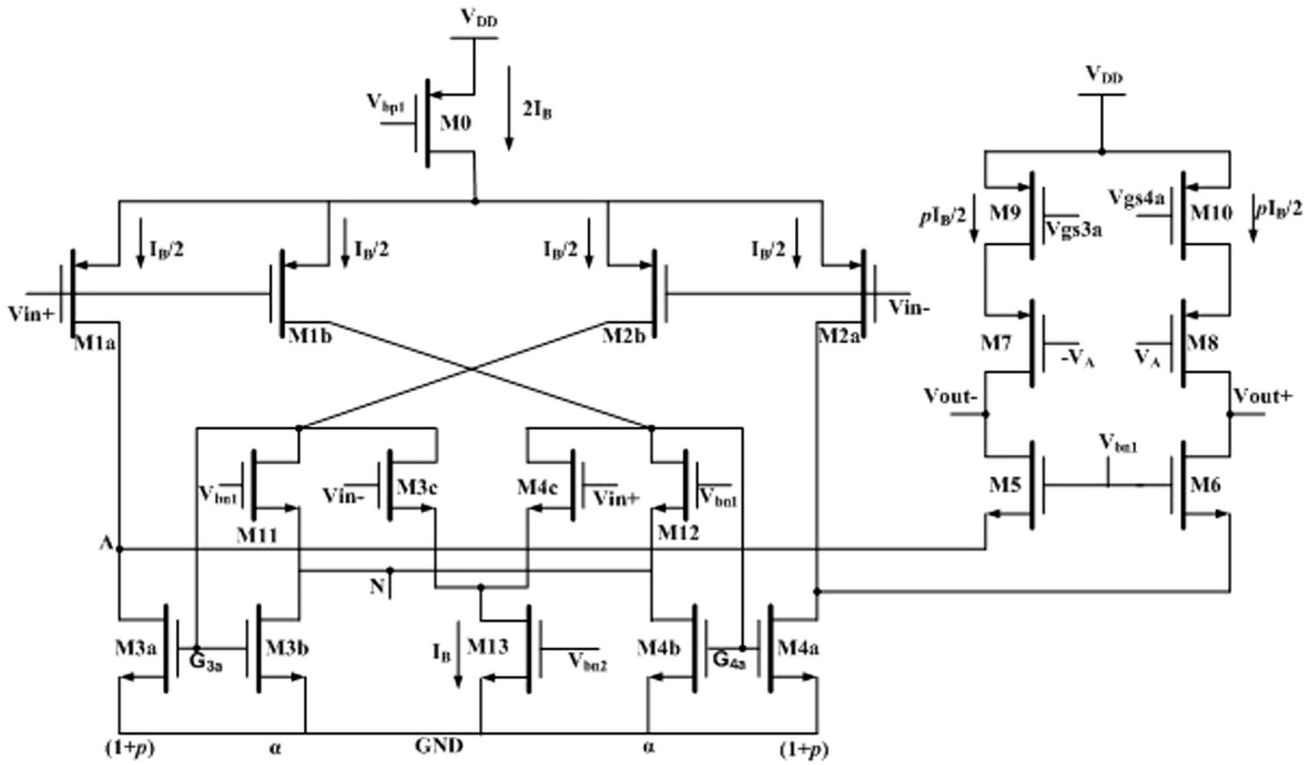

Fig. 4 Proposed enhanced multipath recycling folded cascode amplifier (EMRFC)

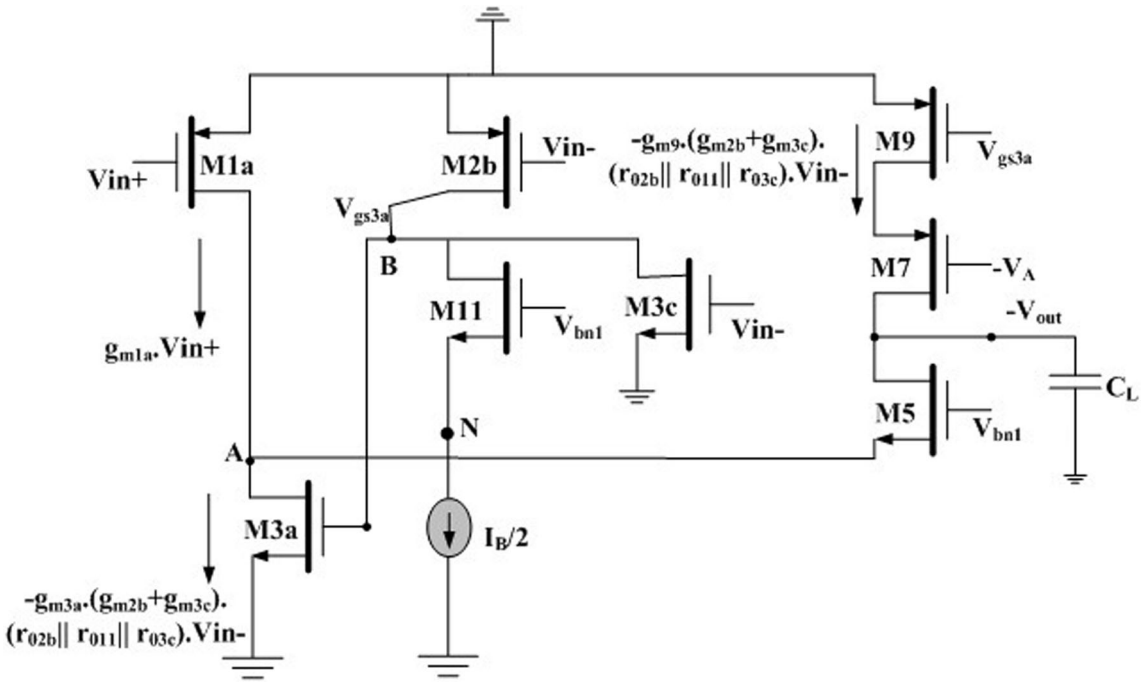

Fig. 5 Half circuit transistor model of EMRFC with effect of node N and multipath recycling

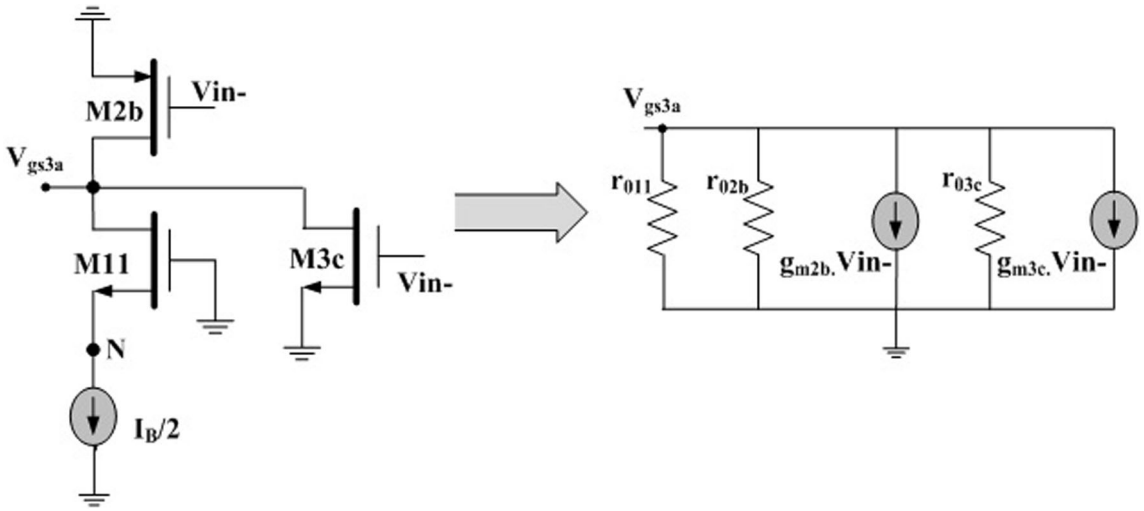

Fig. 6 Section of half circuit transistor model of EMRFC for calculating V_{gs3a}

$$\begin{aligned} I_{SC} &= I_{sd1a} - I_{ds3a} + I_{sd9} \\ &= g_{m1a}.V_{in}^{+} \\ &+ g_{m3a}.V_{in}^{-}.(g_{m2b} + g_{m3c})[r_{02b} \parallel r_{03c} \parallel r_{011}] \\ &+ g_{m9}.V_{in}^{-}.(g_{m2b} + g_{m3c})[r_{02b} \parallel r_{03c} \parallel r_{011}] \end{aligned} \tag{6}$$

Hence the effective transconductance of the proposed EMRFC amplifier after substituting the current ratios as discussed earlier in Eq. (6) is,

$$G_{m,EMRFC} = g_{m1a}.(g_{m2b} + g_{m3c})(1 + 2p).R_X \tag{7}$$

where $R_X = (r_{02b} \parallel r_{03c} \parallel r_{011})$

Out of Eq. (7), it can be concluded that, relative to traditional equivalents FC, RFC and IRFC OTAs, a substantial improvement in the transconductance of the proposed amplifier resulting in an increase of 30-40 dB in the DC gain is likely.

3.1.2 Output impedance

The output impedance of the proposed amplifier is enhanced by adopting positive feedback at the output as shown in Fig. 4. Positive feedback is applied by driving the gate terminals of M7 and M8 output cascode transistors from the folded node. To calculate the output impedance, an arbitrary voltage V_X is applied at the output and the current I_X is measured with input made to zero volts. The half circuit transistor model and its small-signal equivalent for deriving the expression of the output impedance of the proposed EMRFC amplifier is shown in Fig. 7.

From Fig. 7, the output impedance can be expressed as,

$$R_{out,EMRFC} = r_{07}(g_{m7} + g_{mb7})[r_{09} \parallel (r_{03a} + r_{09})] \tag{8}$$

From Eq. (8), it is found that the output impedance of the proposed EMRFC amplifier is enhanced compared to conventional FC, RFC, and IRFC OTA. With these modifications, a DC gain of around 10-15 dB enhancement is likely to achieve compared to its counterparts.

The low frequency gain of any operational transconductance amplifier (OTA) is expressed as the product of effective transconductance and its output impedance. Hence the DC gain of the proposed EMRFC amplifier can be obtained from Eq. (7) and Eq. (8) as,

$$\begin{aligned} A_{V,EMRFC} =& g_{m1a}.(g_{m2b} + g_{m3c})(1 + 2p).R_X \\ & .r_{07}(g_{m7} + g_{mb7})[r_{09} \parallel (r_{03a} + r_{09})] \end{aligned} \tag{9}$$

where g_{mi} is the transconductance of transistor m_i and r_{0i} is the drain to source resistance of the corresponding transistor m_i and $R_X = (r_{02b} \parallel r_{03c} \parallel r_{011})$.

3.1.3 Frequency response

The frequency response of the proposed EMRFC amplifier can be derived by considering its high-frequency model. It can be observed that the proposed EMRFC amplifier exhibits the dominant pole, P_1 at the output node with output capacitance approximately equivalent to load capacitance (C_L). The expression of the dominant pole is given by Eq. (10) as,

$$P_1 = \frac{1}{R_{out}.C_{out}} \approx \frac{1}{R_{out,EMRFC}.C_L} \tag{10}$$

where $R_{out,EMRFC}$ is the output impedance of the proposed amplifier expressed by Eq. (8).

Similarly, the proposed amplifier exhibits two non-dominant poles P_2, and P_3 one at the gate node of recycling current mirror transistor M3a and another one at the folded

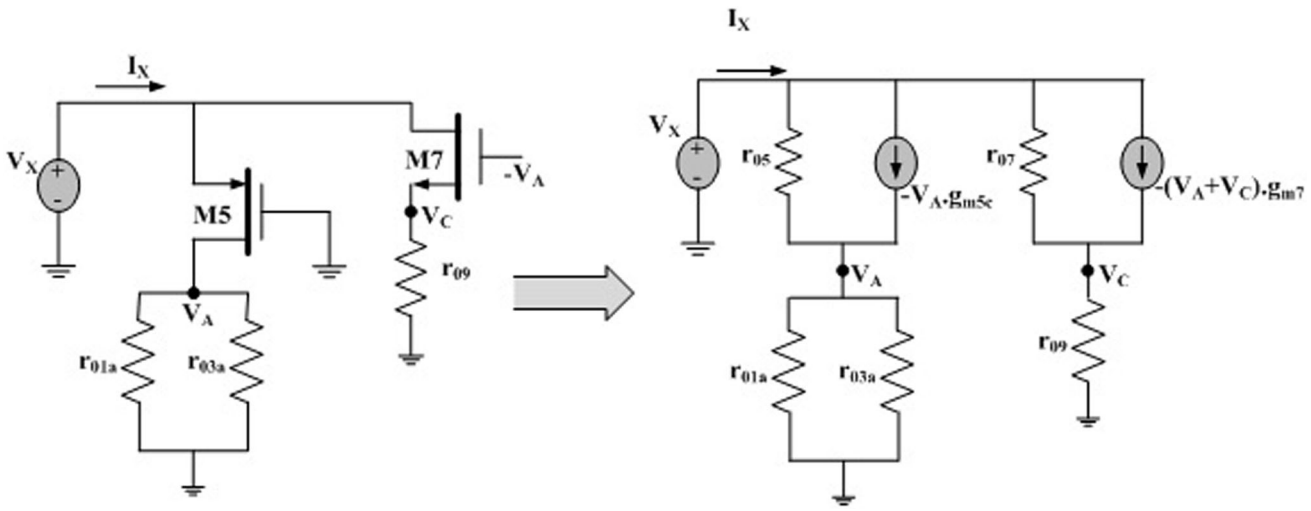

Fig. 7 Equivalent model for output impedance calculation of EMRFC using positive feedback structure

node respectively. The expressions for these two non-dominant poles P_2 and P_3 are given in Eq. (11) and Eq. (12) as,

$$P_2 \cong \frac{1}{\left(r_{02b} \parallel r_{03c} \parallel \left(r_{03b} \parallel \frac{1}{g_{m3b}}\right)\right).C_{gs1a}} \tag{11}$$

$$P_3 \cong \frac{1}{\left(r_{01a} \parallel r_{03a} \parallel \frac{1}{g_{m5}}\right).C_{gs5}} \approx \frac{g_{m5}}{C_{gs5}} \tag{12}$$

The proposed amplifier also exhibits a zero because of the feed-forward path from input to output through the gate-drain capacitance C_{gd} of input transistor M1a, and can be expressed by Eq. (13) as,

$$Z_1 \cong \frac{g_{m1a}}{C_{gd1a}} \tag{13}$$

The unity-gain bandwidth (UGB) of the proposed amplifier can be defined as the product of DC gain given by Eq. (9) and dominant pole frequency given by Eq. (10) and is expressed as,

$$UGB = A_{V,EMRFC}.P_1 \cong \frac{g_{m1a}.(g_{m2b} + g_{m3c})(1+2p).R_X}{C_L} \tag{14}$$

where $R_X = (r_{02b} \parallel r_{03c} \parallel r_{011})$.

Hence from Eq. (14), it can be observed that the suitable selection of p will result in enhanced UGB compared to conventional FC, RFC, and IRFC for the same given current and load capacitance.

As given by Eq. (11) and Eq. (12), the poles P_2, P_3 at the recycling current mirror node and folded node is related to NMOS transistors, hence should be located at a relatively high frequency. When compare to the poles of conventional FC, RFC, and IRFC at these nodes, the poles P_2, and P_3 of the proposed amplifier are at lower frequencies. But because of the increased impedance at the recycling node i.e. at the gate of transistor M3a as shown in Fig. 4 results in a limitation related to the second pole P_2 of EMRFC. Hence this pole P_2 may disturb the dominant pole located at the output by moving to the frequencies less than the dominant pole. Therefore, the proposed EMRFC should be compensated to cancel the effect of this pole P_2 to improve phase margin. A simple RC compensation (Yosefi 2019) can be performed by connecting a resistor R in series with a capacitance C between the output node and the recycling current nodes at the gates of M3a and M4a transistors. Further, the resistors of the compensation circuit can be implemented by using simple pseudo transistors MP1 and MP2 that operate in the triode region, and the same is illustrated in Fig. 8.

The proper selection of R and C values will decrease the impedance at recycling nodes because, at high frequencies, the capacitor C provides a low impedance between outputs ($V_{out+,-}$) and gates of M3a-M4a moving the pole P_2 to high frequencies.

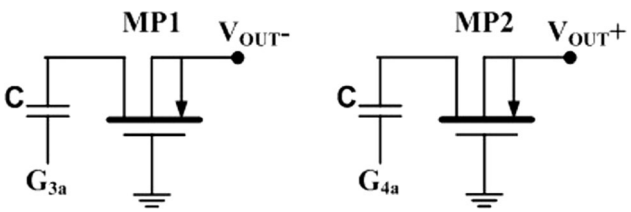

Fig. 8 RC compensation circuit employed in EMRFC between the outputs and nodes G3a and G4a

3.1.4 Slew rate

Slew rate (SR) is one of the main parameters used to study the settling time performance of the OTA. It is defined as the maximum rate of change of voltage to unit time at a given node within the circuit. Slew rate measures, how fast the circuit converts the input to output. Hence for a given amplifier, the higher is the slew rate faster will be the amplifier. A general approach for measuring the slew rate is to apply a large signal at the input and finding the current that charges and discharges the load capacitance.

Slewing process of the proposed EMRFC can be studied as follows: A large positive step input signal is applied at the inputs. When the input V_{in}^{+} goes high, the input transistors M1a and M1b are forced to turnoff which in turn drives the transistors M4a, M4b, and M6 to cutoff which in turn switches off the transistor M2a. Hence the total tail current $2I_B$ from the transistor M0 is forced to flow through M2b which in turn mirrored to M3a with the current ratio $(1+p):\alpha$ from M3b. Similarly, the current from M2b is mirrored to M9 with a current ratio of $p:1$. Hence M9 source current and M3a sink current flows through the load capacitance C_L resulting in the slewing. The slew rate of the proposed amplifier can be expressed as,

$$SR_{EMRFC} = \frac{(1+2p).2I_b}{\alpha.C_L} \tag{15}$$

From Eq. (15), it may be noted that the slew rate of the proposed amplifier EMRFC is also enhanced as transconductance. Therefore the small signal and large signal performance parameters are enhanced in the proposed EMRFC amplifier compared to conventional FC, RFC, and IRFC architectures from the state of art literatures.

3.1.5 Noise

In recent times, for the implementation of analog systems such as biomedical signal acquisition systems, low noise OTAs plays a crucial role. In an analog circuit, noise is considered as an undesired and random signal that disturbs the circuit performance and should be treated properly. The noise limits the signal in the circuit and tradeoffs with power, speed, and linearity. The noise currents in any analog circuit are classified to be either thermal or flicker noise. The thermal and flicker noise components of the proposed amplifier are found and examined separately. From Fig. 4, the transistors that contribute to the overall noise are M1a–M1b, M2a–M2b, M3a–M3b, M4a–M4b, M3c–M4c, and M9–M10. While the noise contributions from the cascode devices M5–M6, M7–M8, and M11–M12, are negligible. Therefore the input-referred thermal noise components of the proposed EMRFC amplifier is expressed as,

$$\bar{V}_{iT,EMRFC}^{2} = \frac{8k_BT\gamma}{G_{m,EMRFC}^{2}}.\left[g_{m1a} + \left(\frac{1+\alpha+p}{\alpha}\right)g_{m3a} + g_{m9} + \left(\frac{1}{g_{m2b}} + \frac{1}{g_{m3c}}\right).G_{m,EMRFC}^{2}\right] \tag{16}$$

Similarly, the input-referred flicker noise component of the proposed EMRFC amplifier is,

$$\bar{V}_{if,EMRFC}^{2} = \frac{2k_{fp}}{C_{ox}.f.G_X^2}\left[\frac{1}{(W.L)_{1a}} + \frac{k_{fn}}{k_{fp}}.\left(\frac{1}{(W.L)_{3a}} + \frac{1}{(W.L)_{3b}}\right).\left(\frac{g_{m3a}}{g_{m1a}}\right)^2 + \left(\frac{g_{m9}}{g_{m1a}}\right)^2.\frac{1}{(W.L)_9} + \left(\frac{1}{(W.L)_{2b}} + \frac{1}{(W.L)_{3c}}.\frac{k_{fn}}{k_{fp}}\right).G_X^2\right] \tag{17}$$

where $G_X = (g_{m2b} + g_{m3c})(1+2p).R_X$ and $R_X = (r_{02b} \parallel r_{03c} \parallel r_{011})$.

From Eq. (16) and Eq. (17), it can be inferred that, when compared to its counterparts FC, RFC and IRFC, the proposed EMRFC amplifier's improved transconductance results in lower input-referred noise. Further reduction in the input-referred noise can be achieved by proper

Table 1 Amplifier transistors width (μm) for L=500nm

Device	FC	RFC	IRFC	EMRFC
M0	164.1	161.6	156.2	156.2
M1/M2	43.8	–	–	–
M1a/M1b/M2a/M2b	–	11.2	12.2	12.2
M3/M4	29.9	–	–	–
M3a/M4a	–	120	8.3	8.6
M3b/M4b	–	40	1.53	1.53
M3c/M4c	–	–	4.01	10.1
M5/M6	60.1	7.0	16.1	16.1
M7/M8	104.1	110	110	92.19
M9/M10	78.2	80	80	3.7
M11/M12	–	40	–	1.53
M11a/M12a	–	–	1.53	–
M11b/M12b	–	–	4.01	–
M13	–	–	–	8.2

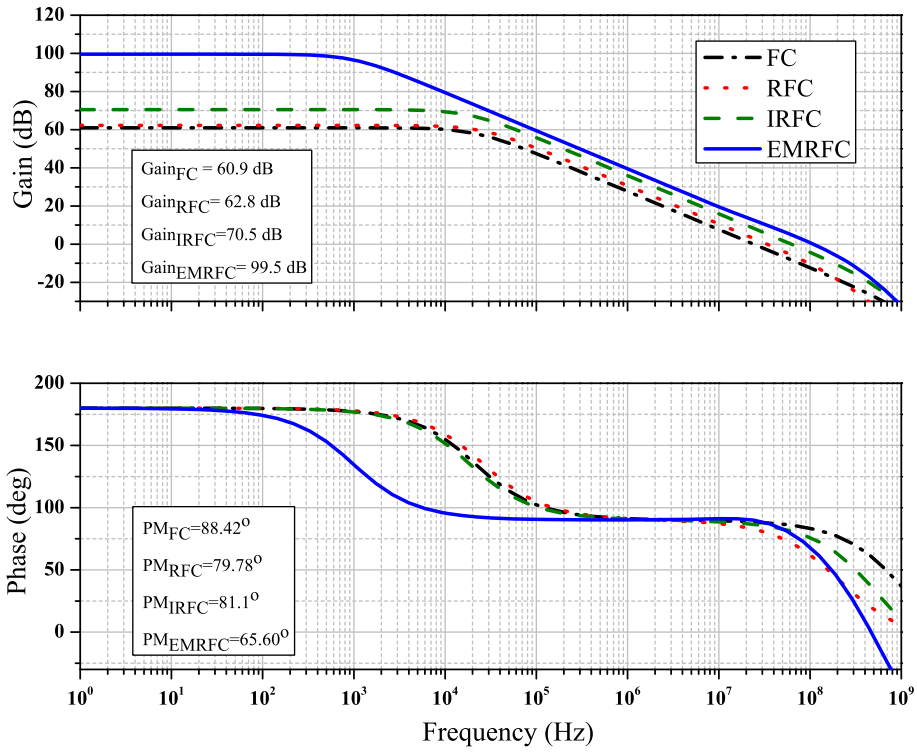

Fig. 9 AC frequency response of FC, RFC, IRFC, and proposed EMRFC amplifiers

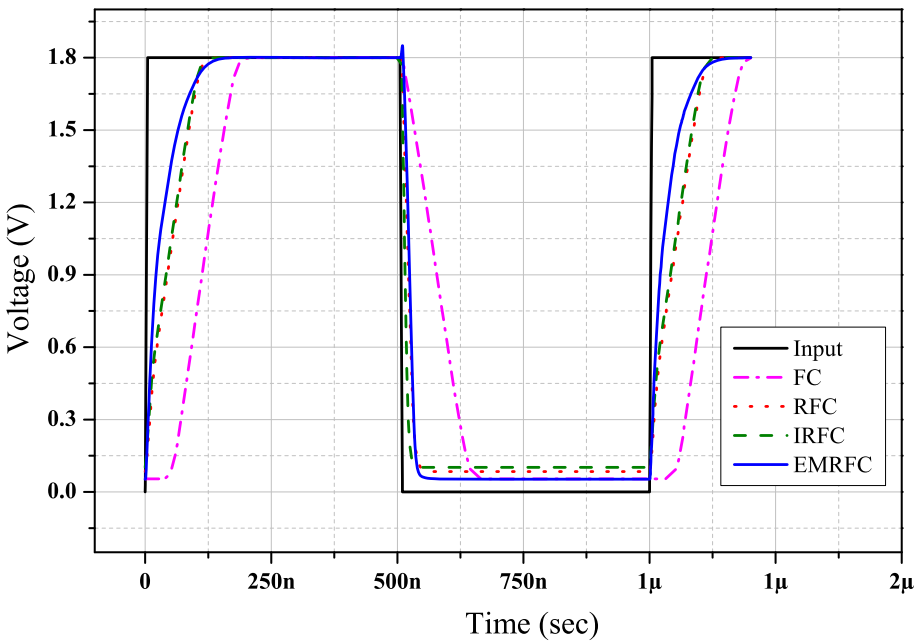

Fig. 10 Small signal step response of amplifiers

selection of p, α, widths, and lengths of the noise contributing transistors.

3.1.6 Offset voltage

Many of the amplifiers exhibit nonzero output voltages even under zero input conditions leading to undesired distortion termed as "offset" which is systematic or random. This limitation of amplifiers is because of either improper selection of circuit topology or due to mismatch and process variations. Hence, to eliminate this distortion, a minimum input voltage is to be applied which is termed as input offset voltage. Pelgrom's mismatch model (Pelgrom et al. 1989) evaluates input offset voltage of any device in terms of its variance because of its random nature and is given by Eq. (18) as,

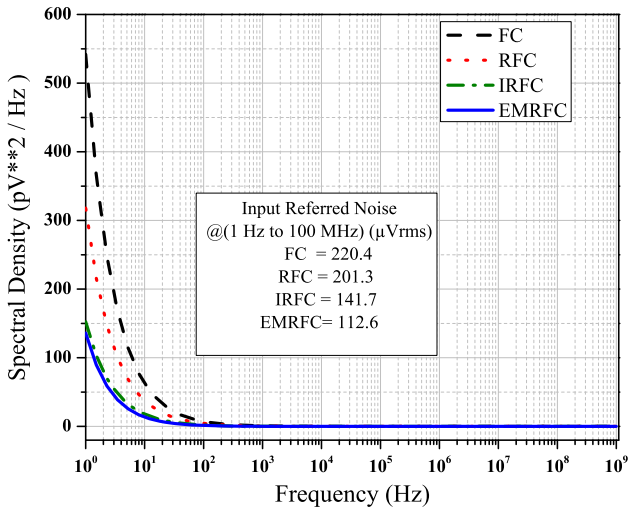

Fig. 11 Spectral density of input referred noise of FC, RFC, IRFC, and proposed EMRFC amplifiers

$$\sigma^2(V_{gs}) = \sigma^2(V_{TH}) = \frac{A_{V_T}^2}{W.L} \tag{18}$$

where A_{V_T} is the area proportionality constant for the threshold voltage V_{TH} and is given by process technology.

The input offset variance of the proposed EMRFC amplifier can be expressed as the sum of drain current variances of all the transistors at the output divided by the effective transconductance of the EMRFC amplifier and is expressed as,

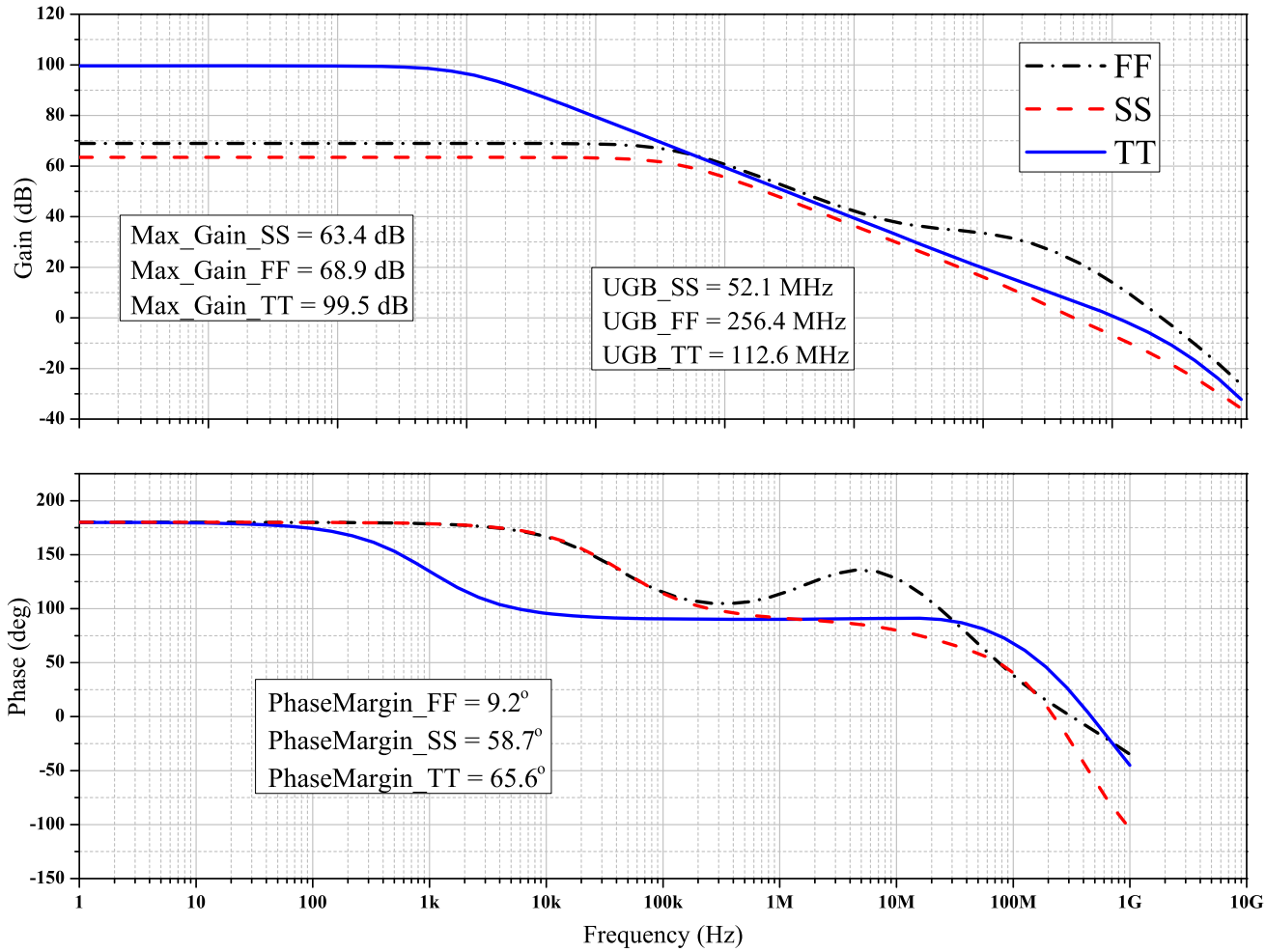

Fig. 12 Frequency response of EMRFC amplifier at various process corners (FF, SS, and TT)

Table 2 Performance comparison of proposed EMRFC OTA with FC, RFC, and RFC OTAs

Parameter	FC	RFC	IRFC	EMRFC
Supply Voltage (V)	1.8	1.8	1.8	1.8
Technology (nm)	180	180	180	180
M1a/M1b/M2a/M2b	–	11.2	12.2	12.2
Current (μA)	300	300	300	300
Capacitive load (C_L)	5	5	5	5
DC Gain (dB)	60.9	62.8	70.53	99.59
Unity gain bandwidth (MHz)	24.6	34.95	64.47	112.6
Phase Margin (^{o})	88.42	79.92	81.27	65.6
Slew Rate (V/μsec)	13.85	40.6	61.2	48.1
Input referred noise (1 Hz–100 MHz) (μV_{rms})	220.48	201.3	141.7	112.6
Input offset voltage (mV)	4.64	4.45	0.045	0.001
FoM_1 (MHz.pF/mA)	410	573.5	1075	1877
FoM_2 (V/μsec.pF/mA)	230.8	676.6	1020	777

Table 3 Variation of performance characteristics at different process corners (SS, FF, and TT) for FC, RFC, IRFC and EMRFC amplifiers

Parameter	Amplifier	SS	FF	TT
DC gain (dB)	FC	33.4	19.9	60.9
	RFC	33.3	50.8	62.8
	IRFC	17.4	14.5	70
	EMRFC	63.4	68.9	99.5
Unity gain bandwidth (MHz)	FC	17.4	29.4	24.6
	RFC	22.4	44.7	34.9
	IRFC	36.1	68.3	64.4
	EMRFC	52.1	256.4	112.6
Phase margin (deg)	FC	89.9	64.6	88.4
	RFC	82.2	80.5	79.8
	IRFC	92.9	93.8	81.2
	EMRFC	58.71	9.20	65.6

$$V_{if,EMRFC}^2 = \frac{2A_{V_{Tp}}^2}{G_X^2}\left[\frac{1}{(W.L)_{1a}} + \frac{\mu_n}{\mu_p}.\left(\frac{L}{W}\right)_{1a}.\frac{A_{V_{Tn}}^2}{A_{V_{Tp}}^2}.\frac{(1+p)(1+p+\alpha)}{\alpha.L_{3a}^2} + \left(\frac{L}{W}\right)_{1a}.\frac{p}{L_9^2} + \left(\frac{1}{(W.L)_{2b}} + \frac{1}{(W.L)_{3c}}.\frac{A_{V_{Tn}}^2}{A_{V_{Tp}}^2}\right).G_X^2\right] \quad (19)$$

From Eq. (19), it can be inferred that the input offset variance of the proposed EMRFC is lower than its counterparts because of enhancement in its transconductance compared to conventional FC, RFC, and IRFC OTAs.

4 Simulation Results

To validate the theoretical results presented so far in the previous sections and to demonstrate the enhancements achieved with the proposed modifications, the proposed EMRFC amplifier with its counterparts FC, RFC, and IRFC is implemented using UMC 180 nm CMOS process technology for a total bias current of 300 μA at a supply voltage of 1.8 V. As illustrated in Figs. 1, 2, and 3, as per the state of art literature the bias currents in FC are in the ratio 1:1, while for RFC it is $k:1$, whereas for IRFC the current splitting ratios are $(1+p):\alpha(1-p):\beta(1-p)$. The current splitting ratio of the proposed EMRFC amplifier as shown in Fig. 4 is $(1+p):\alpha$. To achieve proper biasing conditions, the values of k, p, α, β for RFC and IRFC amplifiers are considered to be 3, 0.5, 0.5, and 0.5 respectively, whereas for EMRFC p, and α are selected to be 2 and 0.5 respectively. For ease of implementation, the length of all the transistors is selected to be 500 nm (Mal et al. 2011; Raja and Kumaravel 2017). Table 1 demonstrates the device sizes used for the implementation of FC, RFC, IRFC, and EMRFC amplifiers. A load capacitance of 5 pF with a compensation capacitance of 5 pF and resistance implemented by pseudo transistors MP1-MP2 of W/L= 6 µm/1 µm that operates in triode region are used for simulation.

The AC frequency response of FC, RFC, IRFC, and proposed EMRFC amplifiers are illustrated in Fig. 9. From the simulations, it is observed that the proposed amplifiers

Table 4 Performance comparison of proposed EMRFC amplifier with state of art literatures

	Assaad and Silva-Martinez (2009)	Yilei et al. (2012)	Akbari et al. (2014)	Kumaravel and Venkataramani (2014)	Yan et al. (2012)	Venishetty and Sundaram (2019)	Yosefi (2019)	Venishetty and Sundaram (2020)	Proposed EMRFC
Supply voltage (V)	1.8	1.2	1.2	1.2	1	1.8	1.8	1.8	1.8
Technology (nm)	180	130	180	90	65	180	180	180	180
Current (μA)	800	300	300	560	800	300	1200	1200	300
Power (μW)	1440	360	360	672	800	540	2160	2160	540
Load capacitor (pF)	5.6	5.5	5	5.6	10	5	5	5	5
DC gain (dB)	60.9	64.9	65.5	62	54.5	76.24	73	79.47	99.59
Unity gain bandwidth (MHz)	134.2	76.2	146.9	164	203.2	74.71	247	285.8	112.6
Phase margin (^{o})	70.6	72.7	81.1	50	66.2	74.41	71	77.12	65.6
Input referred noise (μV_{rms})	48.5	98.5	51.6	–	25.8	139.2	137	185.4	112.6
Input offset voltage (mV)	7.6	–	–	–	–	5.9	1.83	0.07	0.001
Area (μm^2)	4958.2	1139	691	–	–	2760	725	–	5391
FoM_1 (MHz.pF/mA)	939.4	1228.3	2448	-	2540	1245	1029	1191	1877
FoM_2 ($V/\mu sec$.pF/mA)	658.7	379.5	1155	393	878.5	1067.5	525	809.1	777

exhibit a maximum DC gain of 99.59 which is about 40 dB larger than conventional FC OTA, about 37 dB greater than RFC, and around 20 dB larger than IRFC OTAs. Hence the enhancements achieved in transconductance and output impedance as per Eqs. (7) and (8) with the modifications proposed is validated. Further, it can also be observed that the unity-gain bandwidth of the EMRFC amplifier is 112.6 MHz, compared to FC, the UGB of EMRFC is increased by 4.5 times, while the enhancement is about 3.2 times and 1.75 times compared to RFC and IRFC amplifiers respectively which validates the Eq. (14). The phase margins of FC, RFC, IRFC, and EMRFC are found to be $88.4°, 79.9°, 81.2°$, and 65.6^o respectively. The reduction in a phase margin of EMRFC compared to conventional OTAs can be compensated by using simple RC circuits as discussed in previous sections with proper selection of R and C Values.

The slew rate performance of the proposed amplifier can be studied by applying a large signal step of 1.8 V_{PP} at 1 MHz frequency by connecting the amplifier in unity gain mode. The step response of all the amplifiers is illustrated in Fig. 10. The slew rate of FC, RFC, IRFC, and EMRFC amplifiers are found to be 13.85 V/μ sec, 40.6 V/μ sec, 61.2 V/μ sec, and 48.1 V/μ sec. Hence it can be observed that, as stated by Eq. (15), the slew rate of the EMRFC amplifier is increased by 3.5 times and 1.18 times compared to FC and RFC amplifiers respectively.

Noise performance of the proposed amplifier with the conventional OTAs is studied through simulations and the spectral density of all the amplifiers is shown in Fig. 11. The integrated input-referred noise for the frequency range

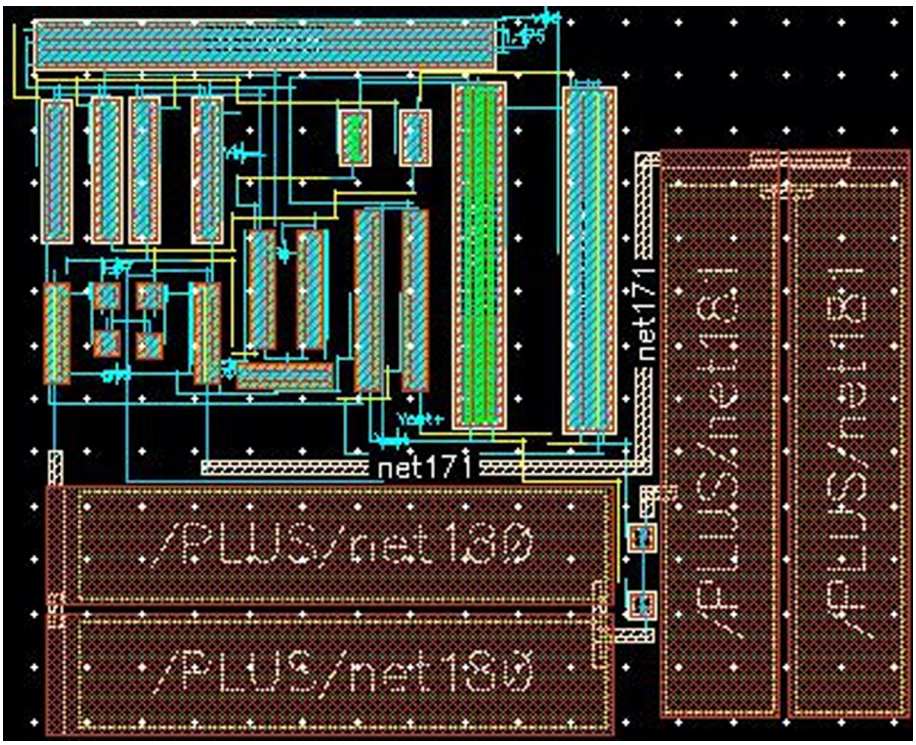

Fig. 13 Layout of the proposed EMRFC amplifier including RC compensation circuit

of 1 Hz to 100 MHz of the proposed EMRFC amplifier is found to be 112.6 μV_{rms}, while it is 220.4 μV_{rms}, 201.3 μV_{rms}, and 141.7 μV_{rms} for FC, RFC, and IRFC amplifiers. The illustrated noise performance confirms the reduction of noise in the proposed amplifier resulted because of enhancement in the transconductance and the same is expressed by Eqs. (16) and (17).

The offset calculation of the proposed amplifier is performed by connecting the amplifier in the unity gain mode and the difference between the two input nodes is measured. The offset voltage of the proposed EMRFC amplifier is found to 1 μV, which is very much smaller than the conventional OTAs.To study the performance of the proposed EMRFC amplifier under process variations, the AC frequency response of the proposed EMRFC amplifier at various process corners SS, FF, and TT is simulated and is illustrated in Fig. 12.

The performance comparison of the proposed EMRFC amplifier with FC, RFC, and IRFC OTAs is illustrated in Table 2. For the purpose of comparison, the simulated results are studied using two figure of Merits FoM_1 and FoM_2 and are expressed by using Eqs. (20) and (21) as,

$$FoM_1 = \frac{GBW.C_L}{I_D} \tag{20}$$

$$FoM_2 = \frac{SR.C_L}{I_D} \tag{21}$$

Table 3 illustrates the variation of performance characteristics at different process corners for FC, RFC, IRFC, and EMRFC amplifiers, while the performance comparison of the proposed EMRFC amplifier with the state of art literature is shown in Table 4. From Table 2 and 4, it can be inferred that the proposed amplifier exhibits high FoMs compared to FC, RFC, IRFC, and other OTAs. The layout of the proposed amplifier is illustrated in Fig. 13 and it occupies an area of 5391 μm^2.

5 Conclusion

Enhanced multipath recycling folded cascode (EMRFC) operational transconductance amplifier (OTA) is presented in this paper. Design and theoretical analysis of the proposed amplifier is done for the performance parameters namely transconductance, DC gain, unity gain bandwidth, slew rate, noise, and input offset voltage. For comparison, the proposed EMRFC amplifier with conventional FC, RFC, and IRFC amplifiers are simulated using UMC 180 nm process technology in a cadence spectre environment. From the simulation results, it is observed that the proposed amplifier exhibits enhance transconductance, DC gain, unity gain bandwidth, noise, and input offset voltage performance compared to conventional OTAs from the state

of art literature. Since the proposed amplifier exhibits reduced input-referred noise compared to FC, RFC, and IRFC amplifiers, this can be used as a preamplifier in biomedical applications.

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Efficient method to identify hidden node collision and improving Quality-of-Service (QoS) in wireless sensor networks

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ABSTRACT

The proposed approach is designed to boost the IEEE 802.15.4 / ZigBee-based WSN streaming efficiency by introducing multipurpose routing. We investigate how those networks can be designed in order to achieve optimum throughput using computational models to explain intra-track and inter-track interference in multipath routing networks. One mode of action in particular – Spatial-TDMA (S-TDMA), Zig Bee dependent WSNs, will greatly reduce the amount of interference, both in one- and multi-track environments. It is also seen that two-way networks can be stronger than their one-way counterparts by means of deliberately selected implementation parameters. Finally, a greater degree of spatial isolation between the routes used indicates improved average efficiency in multi-path scenarios. The simulation is one of our results.

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1. Introduction

There are various types of WSN implementations and there may be different service standard (quality of service) specifications (QoS)[1]. Both WSN systems, however, benefit from increased network performance, less delay in communication, and longer system life.Inside WSNs, QoS is very difficult due to two major challenges:The normally severe limitations of wsn nodes and the extensive architecture of WSNs, as well as resources, networking and computational capabilities.Fig. 1.Fig. 2.

The most interdependent QoS properties will degrade any one of them.This occurs in wireless networking, where a node from a wireless access port, but not from other nodes attached to that access point, is accessible (AP). WLAN refers to nodes beyond all nodes or group of nodes. A loop point of entry through a certain location with many nodes. Nodes cannot communicate with each other because nodes have no physical connection, but each node is different from the AP. In addition, RTS/CTS packages measure the profitability of a traffic segment[3]. In comparison with the hidden stations. A radio domain could be a logical split between the network and the information layer linking all the nodes. A transmitted domain may be found in the same LAN segment.

A variety of related computer network aspects which allow for transport in line with special requirements are defined in Service Quality (QoS)[2]. In practise, a vast range of innovations are introduced to make computer networks as useful as mobile networks to support the new technology with even tougher coverage requirements.

The H-NAMe is a simple but efficient mechanical distribution which addresses the hidden node problem in WSNs. H-NAMe is based on a grouping technique, which splits each WSN cluster into un-hidden node groups, then scales into many clusters with the strategy of cluster grouping, without intervening in the transmission between overlapping clusters[6].The test bed demonstrates how sustainable an H-NAMe is to boost network performance and the likelihood that output will be transmitted double the sum of H-NAMe[8]. The downside of the secret node was shown to be a significant disadvantage, which lowered the performance of the wireless network[5].The use of wireless/mobile networking can benefit tremendously or impose industrial applications, including plant automation, project management and quality control. When virtual networks appear to be universal, largely distributed and embedded into their physical environments [7], all things are continuously tracked and managed everywhere.To be

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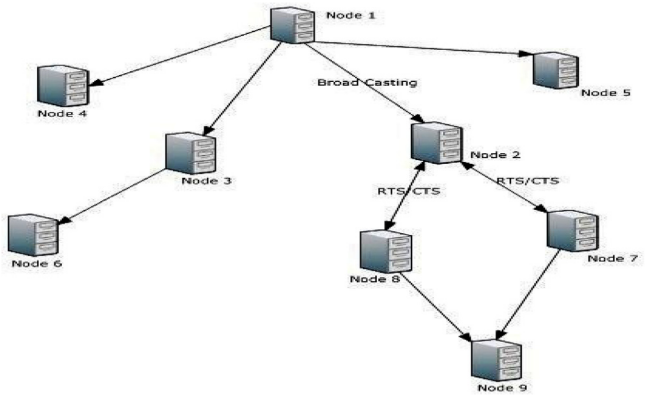

Fig. 1. System Architecture.

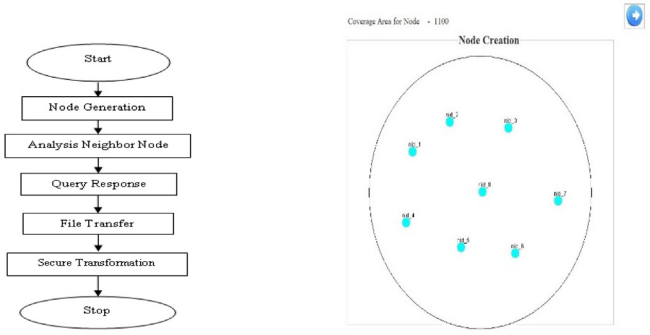

Fig. 2. Data flow Diagram.

cost-effective, small-scale, must be the main components of such systems[4]. Context analysis is a process in which the environment an organisation exists is analysed. The main subject of environmental scan is the macroatmosphere of the industry. However the whole business atmosphere, the internal and external climate take into consideration the context analysis. This can be an important part of business architecture.

2. System architecture

2.1. Existing system

The Head of Cluster (CH) holds a list of groups for nodes. Following receiving a message from the N node with the list of its two-way neighbours, CA initiates an assignment of a group group, in conjunction with its neighbourhood list and available resources, to theoretically assign the node to a given group. Any new node joining the network does not know the node groups and causes a hidden node crash [10].

The key goal is to design a mechanism using an established model, which is the paradigm of groupings in a way:

- It addresses the dilemma of the secret node in multimedia networks
- The protocol stack will be introduced and built-in.
- Returns compatibility with these requirements for the protocol.

2.2. Proposed system

The Head of Cluster (CH) holds a list of groups for nodes. Following receiving a message from the N node with the list of its two-way neighbours, CA initiates an assignment of a group group, in conjunction with its neighbourhood list and available resources, to theoretically assign the node to a given group. Any new node joining the network does not know the node groups and causes a hidden node crash [10].

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- It addresses the dilemma of the secret node in multimedia networks
- The protocol stack will be introduced and built-in.
- Returns compatibility with these requirements for the protocol.

3. Group assignment algorithm

There are a number of nodes and a number of paths. Any node can be assigned to perform any path, incurring some cost that may vary depending on the assignment [5]. It is required to perform all paths by assigning exactly one node to each path in such some way that the overall price of the assignment is reduced [10].

3.1. Data flow Diagram

- Node Generation
- Analysis of Neighbor Node
- File Transfer
- Query response
- Secure transformation

3.1.1. Node generation

A node can be an organisation, a delivery purpose or a terminus of communication. The node description depends on the above-mentioned network and protocol layer. An operational electronic system connected to the network is a physical network node that can trigger, receive or transmit information through a channel of communication. A MAC address must be included for each LAN or WAN node, normally for each network interface controller it has.

A tree can be retrospectively identified as a node array where each node is a value-consistant data structure with a list of nodes that does not repeat any node. Interior nodes are equipped with a variable number of child nodes within a predefined set. The number of children nodes changing as data is added or discharged from a node. Internal nodes can even be connected or broken to preserve the predefined set.

3.1.2. Analysis Neighbor node

In a finite element context, it is often useful to have fast access to the objects which are "around" a certain node. This can be achieved by storing on each node the list of all of the nodes and elements which are close to it. The creation of a list of neighbor nodes and elements implies a no negligible price in terms of memory occupation [9]. A method is provided so as to ease the generation of the lists once required. Neighbor-joining takes as input a distance matrix specifying the space between every combine. The algorithm starts with a totally unresolved tree, whose topology corresponds to it of a star network.

3.1.3. File transfer

Data sharing is a common concept used in a data network such as the internet to transmit information. Many ways to relay file over a network are possible and Protocols are available. Computers that offer a file sharing facility are commonly referred to as file servers. The data transfer is called uploading or copying, depending on

the viewpoint of the user. Data transfer is becoming more and more carried out for the business using File Transfer Controlled.

3.1.4. Query response

The response will be given by the responder to the sower after that the sower will be forwarded that message to the initiator. If the initiator confirms that the response message then the sower will forward that to the responder, hence the sower acts an agent between the initiator and the responder. The answer and forecast response are the values of the dependent variable determined by regression parameters and the experimental variable's value. However, the values of the two answers are the same, their measured variances vary entirely.

3.1.5. Secure transformation

Following a clarification from the initiator, the requested file would then be transmitted via the sower to the respondent. The design of systems which require rigorous handling of doable disrupting sources, ranging from natural catastrophes to malicious actions. Its key aim is to facilitate the supply of software solutions to fulfil pre-defined practical and customer specifications, with an additional layer to avoid abuse and malicious behaviour. it is like most device engineering companies.

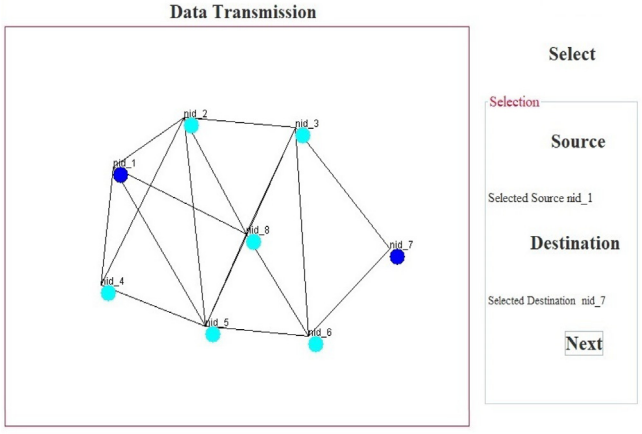

Fig. 3. Node Creation with Coverage Area.

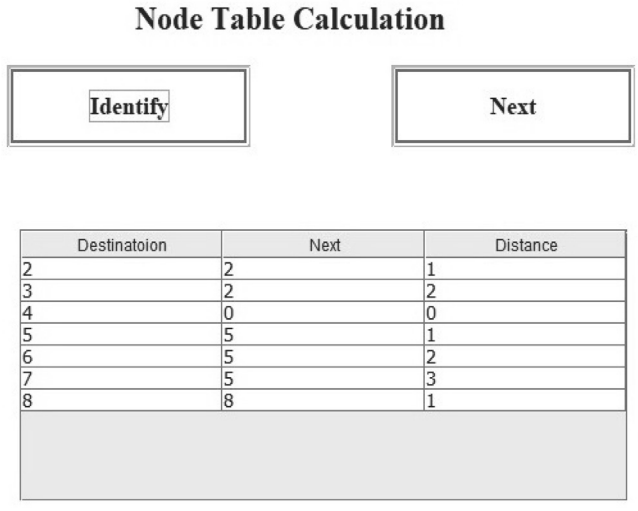

Fig. 4. Data transmission from source node to destination node.

4. Simulation results

Basically, the deficiency in service quality (QoS) masks the node problem, which in turn impacts network performance, message

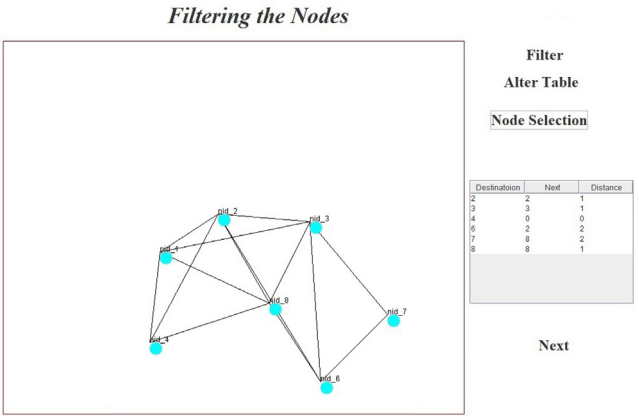

Fig. 5. Distance between a source node to another nodes.

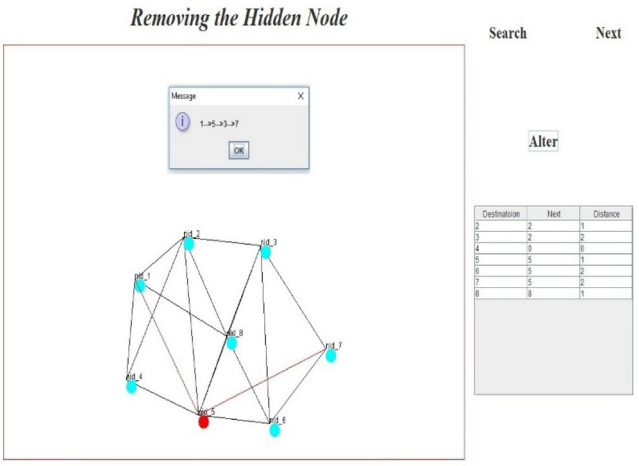

Fig. 6. Detecting shortest path and identify the hidden node.

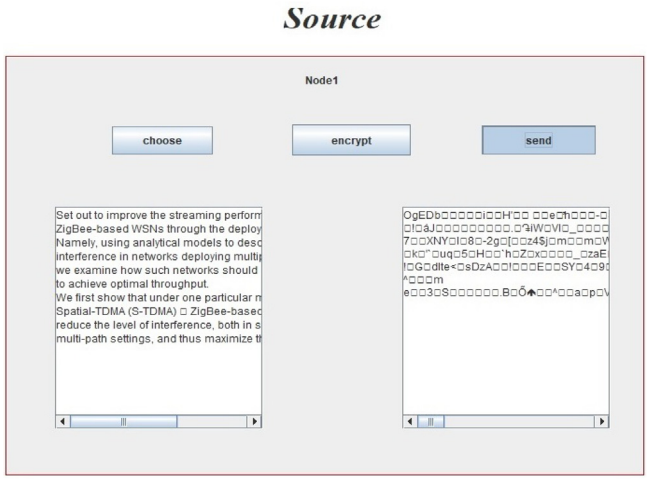

Fig. 7. Removing the hidden node after filtering the nodes.

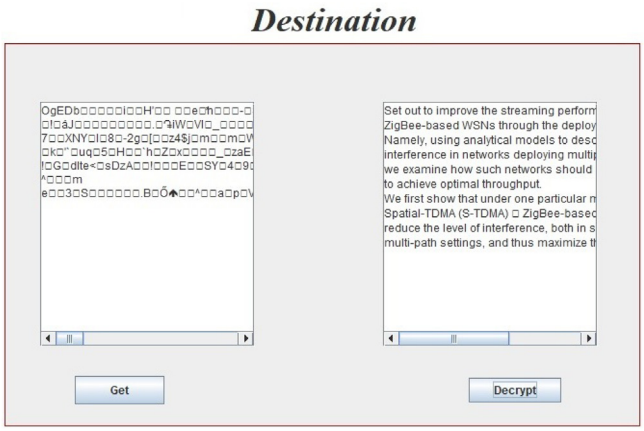

Fig. 8. Source node selects the data file.

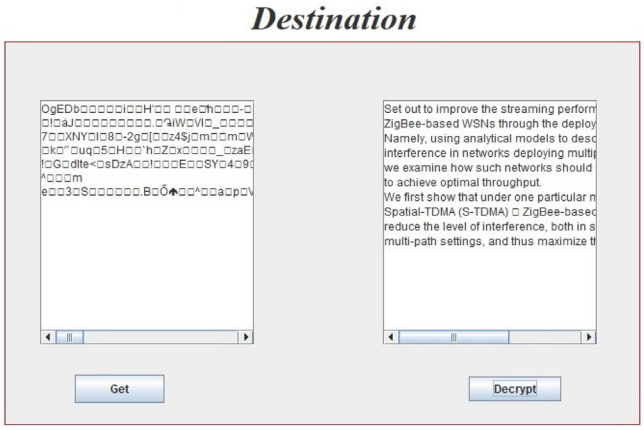

Fig. 9. Destination node received the data file.

latency, consumption of energy and reliability. The System for the Prevention of Secret Nodes (H-NAMe) has been introduced. The first step is that the coverage area must be identified or defined, given the number of nodes in Fig. 3. Pick the source node (node 1) and the destination node (node 7). The next step is to evaluate the surrounding node for data transmission in Fig. 4.

Identify the shortest path that a lead to performance improvement, here the path is 1–5-3–7. But while transferring the data, the hidden node appears and the path is diverted. But the hidden node identified as node 5 is presented in Fig. 6, and the table is depicted in Fig. 5.

This hidden node can be filtered and thus established a clear path between source to destination nodes is presented in Fig. 7. As a final verification, before transmitting the data, the data is encrypted and is transmitted is presented in Fig. 9 Thus by filtering the hidden node, the data was received correctly without delay, which indirectly proves that there is no collision occurred during transmission.Fig. 8.

5. Conclusion

We prove that the networks deploying multipath routing achieve greater streaming performance than their linear network counterparts. In particular, it has been demonstrated that multi-path routing can be increase in the overall packet throughput, and thus can be a preferred routing method in WSNs involving data streaming applications. We use of simulations networks deploying multipath routing can provide a significant increase in performance over single-path networks, we have not provided a protocol which automates the process of zone-disjoint path creation and optimal spatial separation for any given network.

A effective, realistic and scalable approach to synchronised WSN clusters. The Group Access time is defined according to the Group ID field which identifies the group node. A simplistic yet effective solution to the hidden node problem, which constitutes a significant impairment of QoS in wireless networks and especially for WSNs. It prevents secret node collisions in synchronised WSNs with containment-based MAC protocols. We are proposing a Hidden-Node Evasive (H-NAMe) method for the prevention of WSNs, very straightforward but extremely effective. This method was proposed to extend the distributed peer-to-peer network, [11] known as the multi-access multi-tone (RI-BTMA) and dual inhabited tone multiple access[12]. (RI-BTMA)

CRediT authorship contribution statement

B. Vijay Kumar: Conceptualization, Methodology, Software, Visualization, Writing - original draft. **Syed Musthak Ahmed:** Data curation, Supervision, Software. **M.N. Giri Prasad:** Validation, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Solid State Technology

Mobility Aware Trust Assessment Multipath Routing (Matar) For Mobile Adhoc Networks

P. Shailaja, Prof. C. V. Guru Rao

Abstract

A Mobile Adhoc Network (MANET) is an autonomous infrastructureless network that is self-organized by mobile nodes communicating with each other dynamically and freely. In such kind of environments, security provision is a challenging task. Due to the mobility, the mobile nodes moves out and in of radio frequency range which results in the link breakages followed by packet drops. For a packet drop, confusion will arise whether it was happened due to mobility or due to compromised node and results is more number of false positives and less Quality of Service. To overcome these problems, in this paper, a new routing mechanism called as Mobility Aware Trust Assessment Routing (MATAR) is proposed. In MATAR, each node measured its neighbor node's trustworthiness with respect to its packet forwarding history. Both direct and recommended trusts are evaluated here and also linked the total trust with the mobility of respective node. In this approach, the route trust is computed by the integration of individual intermediate node's trustworthiness. Further, a trust application is defined with respect to five node classes which helps in the provision of an alternative nodes and results in the QoS preservation. An extensive Simulation experiments are performed over the proposed model and the performance is measured through Malicious Detection Rate, Throughput and Routing Overhead. The results show that the MATAR improves the Quality of Service along with accurate detection of malicious nodes.

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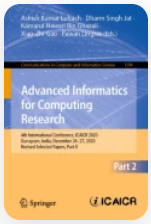

Advanced Informatics for Computing Research

(ICAICR 2020)

Kalyanapu Srinivas, V. Janaki, V. Shankar & P. KumarSwamy

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Abstract

Cryptography is a mechanism used for protection of valuable information from unacceptable users in the networking world. It's a challenging task to protect such assets from illegal users. This necessitated for the development of Cryptographic techniques to provide security as large volumes of digital data traveling through the shared media. These techniques range from traditional security systems to crypto image techniques. This brings forward to focus on cryptographic techniques that have strong algorithm and strong key. The strength of any crypto algorithm depends on the strongness of the crypto key used. Therefore, both the algorithm technique and key generation methodology are equally important. This motivated to propose and concentrate on a novel scheme that includes crypto key generation and crypto key protection where the protected key and its methodology cannot be traced by an ineligible user.

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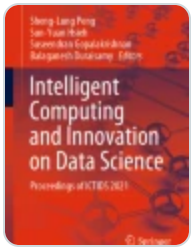

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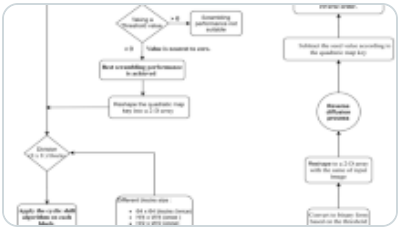

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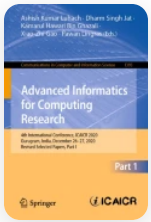

Advanced Informatics for Computing Research

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Nimmala Mangathayaru, B. Padmaja Rani, V. Janaki, Shilhora Akshay Patel, G. Sai Mohan & B. Lalith Bharadwaj

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Abstract

Cardiovascular disease are one of the leading causes of an increase in the mortality rate due to irregular heart beats. Photoplethysmogram (PPG) technique is one of the noninvasive evaluation of blood pressure (BP) offers a reliable, feasible, and cost-efficient solution than other conventional techniques. PPG technique is highly induced by motion artifacts and its characteristics depend on the physiological condition of the person. While the collection of data, the PGG must be calibrated. In this research, a novel approach using a dual-tree complex wavelet transform (DT-CWT) based feature extraction technique with GRU network for the classification of hypertension is proposed. DT-CWT gives shift invariance compared to Continuous wavelet transforms and dual tree structure helps to extract the real and imaginary coefficients of the features. DT-CWT helps to integrate the signal patterns even disintegrating them during testing procedure. Further, these extracted features are fed into a variant neural architecture consisting of sequential GRU layers stacked over fully connected dense layers. It is observed, utilizing GRU layers led to extract precise features for sequential signal data by out-performing existing models. The proposed model attained an state-of-the-art accuracy score of 98.82% on BIDMC-PGG dataset by overhauling existing loops in research.

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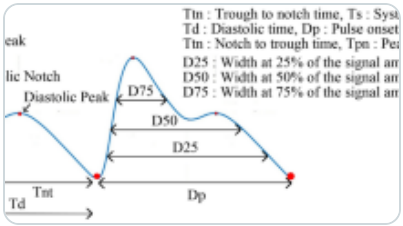

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An Experimental Approach of Machine Learning Algorithms to Detect Botnet DDoS Attacks

Voore Subrahmanyam, Vinnakota Shivani, Siraboina Prasunanju, Akula Pranay, Sanikommu Shreya Reddy

Abstract

Botnets are one of the threats in a network to hamper the quality of the network by disrupting theresources of the network. These Botnets can be controlled remotely by Botmaster. The Machine Learning Algorithms play a major role to detect and control the Botnets that cause to DDoS attacks, malwares and phishing attacks that are vulnerable to network resources. The DDoS attacks are most dangerous malware events that disrupt whole network. To solve DDoS attacks, various methods and algorithms are proposed. In this study, we proposed K-means Unsupervised Learning (USML) algorithm. In the proposed methodology, we conduct a practical approach, analyzing by ML algorithms i.e., K-means algorithms for the detecting Botnet DDoS attacks. For experimental analysis, we consider the UNBS-NB real-time datasets. In this approach, we compare K-means algorithms with Support Vector Machine (SVM), Artificial Neural network (ANN), Naive Bayes (NB) and Decision Tree (DT) for performance-based comparison. In results, we find that K-means (USML) is showing better performance than other machine learning algorithms.

Keywords

Botnet, Distributed Denial of Service (DDS) attacks, machine learning algorithms, Kmeans algorithm

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